Joseph Devietti

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Research Interests

My main research interests are in the fields of computer architecture and programming languages. I'm interested in using language and hardware innovations to provide better support for parallel programming.

Employment

University of Pennsylvania, 2013-present
Assistant Professor, Department of Computer & Information Science

Education

University of Washington, 2012
PhD in Computer Science and Engineering, advised by Luis Ceze and Dan Grossman

University of Washington, 2009
Master of Science in Computer Science and Engineering

University of Pennsylvania, 2006
Bachelor of Science in Engineering degree in Computer Science and Bachelor of Arts degree in English. Graduated magna cum laude.

Honors & Awards

- 2013 Intel Early Career Faculty Honor Program
- 2011 Intel Ph.D. Fellowship
- Paper selected for IEEE Micro *Top Picks in Computer Architecture from 2009*
- Paper selected for IEEE Micro *Top Picks in Computer Architecture from 2008*
- Eta Kappa Nu Engineering Honor Society, University of Pennsylvania
- Benjamin Franklin Scholar, University of Pennsylvania

Students

- Christian DeLozier (PhD)
- Sana Kamboj (Master's)
- Omar Navarro Leija (PhD)

- Yuanfeng Peng (PhD)
- Nimit Singhania (PhD, co-advised with Rajeev Alur)

Former students

- Ariel Eizenberg (Master's 2016)
- Brooke Fugate (Master's 2015, co-advised with André DeHon)
- Liang Luo (Master's 2015, now a PhD student at the University of Washington)
- Akshitha Sriraman (Master's 2015, now a PhD student at the University of Michigan)

Publications

Conference Papers

- *GPUDrano: Detecting Uncoalesced Accesses in GPU Programs*
  Rajeev Alur, Joseph Devietti, Omar Navarro Leija and Nimit Singhania
  International Conference on Computer-Aided Verification *(CAV '17)*, July 2017

- *BARRACUDA: Binary-level Analysis of Runtime RAces in CUDA programs*
  Ariel Eizenberg, Yuanfeng Peng, Toma Pigli, William Mansky and Joseph Devietti
  ACM SIGPLAN Conference on Programming Language Design and Implementation *(PLDI '17)*, June 2017

- *Remix: Online Detection and Repair of Cache Contention for the JVM*
  Ariel Eizenberg, Shiliang Hu, Gilles Pokam and Joseph Devietti
  ACM SIGPLAN Conference on Programming Language Design and Implementation *(PLDI '16)*, June 2016

- *LASER: Light, Accurate Sharing dEtection and Repair*
  Liang Luo, Akshitha Sriraman, Brooke Fugate, Shiliang Hu, Gilles Pokam, Chris Newburn and Joseph Devietti
  IEEE International Symposium on High Performance Computer Architecture *(HPCA '16)*, March 2016

- *Co-Design of Anytime Computation and Robust Control*
  Yash Pant, Kartik Mohta, Houssam Abbas, Truong X. Nghiem, Joseph Devietti and Rahul Mangharam
  IEEE Real-Time Systems Symposium *(RTSS '15)*, December 2015

- *High-Performance Determinism with Total Store Order Consistency*
  Timothy Merrifield, Joseph Devietti and Jakob Eriksson
  European Conference on Computer Systems *(EuroSys '15)*, April 2015

- *GPUDet: A Deterministic GPU Architecture*
  Hadi Jooybar, Wilson W. L. Fung, Mike O'Connor, Joseph Devietti and Tor Aamodt
  International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS '13)*, March 2013

- *RADISH: Always-On Sound and Complete Race Detection in Software and Hardware*
  Joseph Devietti, Ben Wood, Karin Strauss, Luis Ceze, Dan Grossman and Shaz Qadeer
  International Symposium on Computer Architecture *(ISCA '12)*, June 2012

- *RCDC: A Relaxed-Consistency Deterministic Computer*
  Joseph Devietti, Jacob Nelson, Tom Bergan, Luis Ceze and Dan Grossman
  International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS '11)*, March 2011

- *CoreDet: A Compiler and Runtime System for Deterministic Multithreaded Execution*
  Tom Bergan, Owen Anderson, Joseph Devietti, Luis Ceze and Dan Grossman
  International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS '10)*, March 2010

- *DMP: Deterministic Shared Memory Multiprocessing*
  Joseph Devietti, Brandon Lucia, Luis Ceze and Mark Oskin
  International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS '09)*, March 2009
  Selected for IEEE Micro Top Picks '09

- *Atom-Aid: Surviving and Detecting Atomicity Violations*
  Brandon Lucia, Joseph Devietti, Karin Strauss and Luis Ceze
  International Symposium on Computer Architecture *(ISCA '08)*, June 2008
  Selected for IEEE Micro Top Picks '08

- *HardBound: Architectural Support for Spatial Safety of the C Programming Language*
  Joseph Devietti, Colin Blundell, Milo Martin and Steve Zdancewic
  International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS '08)*, March 2008

- *Making the Fast Case Common and the Uncommon Case Simple in Unbounded Transactional Memory*
  Colin Blundell, Joseph Devietti, E Christopher Lewis and Milo Martin
  International Symposium on Computer Architecture *(ISCA '07)*, June 2007

Journal Papers

- *DMP: Deterministic Shared-Memory Multiprocessing*
  Joseph Devietti, Brandon Lucia, Luis Ceze and Mark Oskin
  IEEE Micro, Vol. 30 No. 1, January 2010

- *Atom-Aid: Detecting and Surviving Atomicity Violations*
  Brandon Lucia, Joseph Devietti, Luis Ceze and Karin Strauss
  IEEE Micro, Vol. 29 No. 1, January 2009

Workshop Papers

- *Verifying Dynamic Race Detection*
  William Mansky, Yuanfeng Peng, Steve Zdancewic and Joseph Devietti
  Certified Programs and Proofs *(CPP '17)*, co-located with POPL 2017, January 2017

- *MAMA: Mostly Automatic Management of Atomicity*
  Christian DeLozier, Joseph Devietti and Milo Martin
  Workshop on Determinism and Correctness in Parallel Programming *(WoDet '14)*, held in conjunction with ASPLOS '14, March 2014

- *The Case For Merging Execution- and Language-level Determinism with MELD*
  Joseph Devietti, Dan Grossman and Luis Ceze
  Workshop on Determinism and Correctness in Parallel Programming *(WoDet '12)*, held in conjunction with ASPLOS '12, March 2012

- *The Deterministic Execution Hammer: How Well Does it Actually Pound Nails?*
  Tom Bergan, Joseph Devietti, Nicholas Hunt and Luis Ceze
  Workshop on Determinism and Correctness in Parallel Programming *(WoDet '11)*, held in conjunction with ASPLOS '11, March 2011

- *Lock Prediction*
  Brandon Lucia, Joseph Devietti, Tom Bergan, Luis Ceze and Dan Grossman
  USENIX Workshop on Hot Topics in Parallelism *(HotPar '10)*, accepted for poster session, June 2010

- *The Case for System Support for Concurrency Exceptions*
  Luis Ceze, Joseph Devietti, Brandon Lucia and Shaz Qadeer
  USENIX Workshop on Hot Topics in Parallelism *(HotPar '09)*, March 2009

- *Explicitly Parallel Programming with Shared-Memory is Insane: At Least Make it Deterministic!*
  Joseph Devietti, Brandon Lucia, Luis Ceze and Mark Oskin
  Workshop on Software and Hardware Challenges of Manycore Platforms *(SHCMP '08)*, held in conjunction with ISCA '08, June 2008

Posters

- *SlimFast: Reducing Metadata Redundancy in Sound & Complete Dynamic Data Race Detection*
  Yuanfeng Peng and Joseph Devietti
  PLDI Student Research Competition *(PLDI SRC '15)*, held in conjunction with PLDI '15, June 2015

Technical Reports

- *Code-Centric Communication Graphs for Shared-Memory Multithreaded Programs*
  Ben Wood, Joseph Devietti, Luis Ceze and Dan Grossman
  Technical Report UW-CSE-09-05-02, May 2009

Dissertation

- *Deterministic Execution for Arbitrary Multithreaded Programs*
  Joseph Devietti
  PhD Dissertation, University of Washington, November 2012

Invited Talks

- *Automatically Finding & Fixing Cache Contention Bugs*
  Washington University in St. Louis, 18 November 2016
  [abstract]

- *Automatically Finding & Fixing Cache Contention Bugs*
  Carnegie Mellon University, 20 September 2016
  [abstract]

- *Towards Automatic Synchronization of Parallel Programs*
  Qualcomm Research, San Diego, 13 March 2015
  [abstract]

- *Low-overhead, Unobtrusive Cache Contention Detection and Repair*
  Intel Labs, Santa Clara, 6 February 2015
  [abstract]

- *Towards Automatic Synchronization of Parallel Programs*
  Intel Labs, Santa Clara, 7 February 2014
  [abstract]

- *No Such Thing as Luck: Improving Parallel Programming with Determinism*
  Rutgers University, 3 December 2013

- *No Such Thing as Luck: Improving Parallel Programmability with Determinism*
  Microsoft Research, Redmond, 23 April 2012
  [abstract] [video]

- *No Such Thing as Luck: Improving Parallel Programmability with Determinism*
  Penn State, Computer Science & Engineering, 18 April 2012
  [abstract]

Current Funding

- Intel: Leveraging Intel Platforms to Understand and Optimize Full-System Caching Behavior. $75,000, 2016. (PI)
- NSF 1525296: SHF: SMALL: LUCID: Low-overhead, Unobtrusive Cache Contention Detection and Repair. $480,000, 2015-2018. (PI)
- NSF XPS-1337174: CLCCA: Improving Parallel Program Reliability Through Novel Approaches to Precise Dynamic Data Race Detection. $700,000, 2013-2017. (PI with Co-PIs Stephan Zdancewic and Milo Martin)
- Intel Early Career Faculty Award. $40,000.

Teaching

- CIS 601: GPGPU Programming Models (grad-level) — University of Pennsylvania — Spring 2016, Spring 2017
- CIS 501: Computer Architecture (grad-level) — University of Pennsylvania — Fall 2013, Spring 2015, Fall 2015, Fall 2016
- CIS 601: Security in Multicore Architectures (grad-level) — University of Pennsylvania — Spring 2014
- CIS 800-003: Topics in Parallel Programmability (grad-level) — University of Pennsylvania — Spring 2013
- CSE 399: Unix/Linux Skills (undergrad-level) — University of Pennsylvania — Spring 2007

Professional Activities

Organizer

- Co-organizer of the 5th Workshop on Determinism and Correctness in Parallel Programming *(WoDet 2014)*, co-located with ASPLOS 2014
- Co-organizer of the 4th Workshop on Determinism and Correctness in Parallel Programming *(WoDet 2013)*, co-located with ASPLOS 2013
- Co-organizer of the 3rd Workshop on Systems for Future Multicore Architectures *(SFMA 2013)*, co-located with EuroSys 2013

Conference Program Committees

- International Symposium on Code Generation and Optimization *(CGO)* 2017
- ACM SIGPLAN Conference on Programming Language Design and Implementation *(PLDI)* 2017

- International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS)* 2016
- IEEE International Symposium on High Performance Computer Architecture *(HPCA)* 2013, 2014, 2016
- IEEE Micro's Top Picks from the Computer Architecture Conferences *(IEEE Micro Top Picks)* 2016

Conference/Journal Reviewer

- International Conference on Architectural Support for Programming Languages & Operating Systems *(ASPLOS)* 2010-2012, 2017
- ACM IEEE International Symposium on Microarchitecture *(MICRO)* 2013-2017
- IEEE International Symposium on High Performance Computer Architecture *(HPCA)* 2017
- European Conference on Object-Oriented Programming *(ECOOP)* 2017
- ACM Transactions on Parallel Computing *(TOPC)* 2014, 2017
- ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming *(PPoPP)* 2012, 2016
- ACM Transactions on Architecture and Code Optimization *(TACO)* 2012-2016
- International Symposium on Computer Architecture *(ISCA)* 2008, 2013-2015
- IEEE Computer Architecture Letters *(CAL)* 2013, 2015
- ACM SIGPLAN Conference on Programming Language Design and Implementation *(PLDI)* 2011, 2012, 2015
- Transactions on Computer-Aided Design of Integrated Circuits and Systems *(TCAD)* 2015
- Elsevier Science of Computer Programming *(SCP)* 2015
- ACM Transactions on Computer Systems *(TOCS)* 2015
- International Symposium on Code Generation and Optimization *(CGO)* 2014
- International Conference on Parallel Architectures and Compilation Techniques *(PACT)* 2014
- IEEE Transactions on Computers *(TC)* 2013
- ACM Transactions on Programming Languages and Systems *(TOPLAS)* 2013
- IEEE Symposium on Security and Privacy *(Oakland)* 2011
- ACM International Conference on Supercomputing *(ICS)* 2009

Other Reviewing

- PC member for the International Workshop on Dynamic Analysis *(WODA 2014)*, held in conjunction with ISSTA 2014
- PC member for the Workshop on Systems for Future Multicore Architectures *(SFMA 2014)*, held in conjunction with EuroSys 2014
- Poster Session PC member at *EuroSys* 2014
- Poster Session PC member at *SOSP* 2013
- PC member for the Workshop on Transitioning to Multicore, held in conjunction with OOPSLA 2011
- Reviewer for the ACM SIGPLAN Workshop on Memory Systems Performance and Correctness *(MSPC)* 2011
- Reviewer for the International Symposium on Memory Management *(ISMM)* 2009

Other Roles

- Artifact Evaluation Chair of the International Symposium on Code Generation and Optimization (*CGO* 2017)
- Treasurer & Registration Chair of the 21st IEEE Symposium on High Performance Computer Architecture (*HPCA* 2015)

Patents

- Luis Ceze, Thomas Bergan, Joseph Devietti, Daniel Grossman, Jacob Nelson. "Systems and Methods for Providing Deterministic Execution." U.S. Patent No. 9,146,746 issued September 2015.
- Luis Ceze, Mark Oskin, Joseph Devietti, Brandon Lucia. "Critical path deterministic execution of multithreaded applications in a transactional memory system." U.S. Patent 8,739,163 issued May 2014.